

2826



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PTO/SB/21 (08-00)
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Application Number	10/010,343
Filing Date	December 5, 2001
First Named Inventor	Visvamohan Yegnashankaran et al.
Group Art Unit	2826
Examiner Name	L. Andujar
Attorney Docket Number	100-16300 (P05089)

Total Number of Pages in This Submission	2
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ENCLOSURES (check all that apply)		
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Firm or Individual name	Mark C. Pickering, Reg. No. 36,239
Signature	
Date	September 5, 2003

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES PATENT

In re Patent Application of) Group Art Unit: 2826
Visvamohan Yegnashankaran et al.) Examiner: L. Andujar
Appln. No. 10/010,343) ESTABLISHMENT OF RIGHT OF ASSIGNEE
Filed: December 5, 2001) TO PROSECUTE UNDER 37 C.F.R. §3.73(b)
For: INTEGRATED CIRCUIT AND METHOD)
OF FORMING THE INTEGRATED)
CIRCUIT HAVING A DIE WITH HIGH Q)
INDUCTORS AND CAPACITORS)
ATTACHED TO A DIE WITH A CIRCUIT)
AS A FLIP CHIP)

Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

NATIONAL SEMICONDUCTOR CORPORATION is the assignee of the entire right, title and interest in the above-identified application by assignment dated November 29, 2001 and November 28, 2001, **which assignment is recorded in the U.S. Patent and Trademark Office at Reel 012373, Frame 0443.**

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

Dated: 8/25/03

By: 

Name: Christopher J. Byrne

Title: Director of Intellectual Property and Technology
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